REMARKS

Applicant respectfully requests reconsideration of this application. Claims 1-88 are currently pending in this application. Claims 1, 12, 20, 28, 35, 47, 59 are currently amended.

Claim Rejections - 35 U.S.C. §102

The Office Action rejected claims 1-4, 20, and 28 under 35 U.S.C. 102(e) as being anticipated by Hardin (U.S. Patent No. 6,658,043).

The Office Action rejected claims 20, 22-26, 28, 30-33, 35, 37-42, 44-47, 49-54, 59, 61-66, 71-81, and 84-86 under 35 U.S.C. 102(a) as being anticipated by Paist (U.S. Patent No. 6,919,744).

The Office Action rejected claims 35, 41, 47, 53, 59, and 65 under 35 U.S.C. 102(e) as being anticipated by Sha (U.S. Patent No. 6,980,581).

Response to Claim Rejections - 35 U.S.C. §102

Regarding the rejection of claims 1-4, 20, and 28 under 35 U.S.C. 102(e) as being anticipated by Hardin, applicant has amended claims 1, 20 and 28 to overcome the examiner's rejection. Specifically, applicant has amended claim 1 to add the limitation of updating the profile memory in response to changes in nominal frequency, amended claim 20 to add the limitation of obtaining a profile corresponding to a new nominal frequency upon a change in nominal frequency, amended claim 28 to add the limitations that the PLL is capable of adjusting the clock frequency among a plurality of nominal frequencies, together with obtaining a profile corresponding to a new nominal frequency.

Applicant submits that the present invention is not anticipated by Hardin because Hardin fails to teach an element of the invention, which is a profile memory capable of being updated in response to changes in nominal frequency.

Applicant submits that embodiments of the present invention provide the optimization of spreading frequency profile even when the nominal clock frequency changes. For

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digital circuits, the nominal frequency of the clock signal can change in response to the changes in operating conditions. For example, the nominal clock frequency decreases to a lower value for reducing power consumption or heat generation, and increases to a higher value for improved computation performance. The change in nominal clock frequency is thus different than the change in clock frequency due to spreading which is to reduce electromagnetic interference. Different nominal frequency typically requires different spreading profiles for optimizing the electromagnetic interference.

The number of nominal frequencies can be infinitely large, leading to an impractically large memory to store the spreading profiles. Thus in an embodiment reflected in claim 1, the present invention discloses a circuit comprising a profile memory capable of being updated in response to changes in nominal clock frequency. In an exemplary embodiment, the present invention provides a profile when the nominal frequency changes with a finite memory capacity.

In contrast, applicant submits that Hardin discloses a RAM 54 loaded with a particular desired frequency (read nominal frequency) and deviation output (read spreading profile) only after a power-on reset sequence (Col. 8, lines 15-22). Applicant submits that a RAM does not retain its memory, thus needs to be initialized after a power-up or after a reset. Thus the disclosure of Hardin in loading the RAM 54 with a particular desired clock frequency (i.e. nominal frequency) and its deviation output (i.e. spreading profile) is a normal procedure of powering a RAM circuit. Thus applicant submits that Hardin fails to teach that the profile memory can be updated in response to changes in nominal frequency.

Further applicant submits that Hardin discloses an apparatus and method for reducing electromagnetic emission for a circuit employing two fixed nominal clock frequencies. Applicant submits that Hardin is silent with respect to the change in nominal clock frequency, and also silent with respect to the dynamic changing of the spreading profile when the nominal clock frequency changes.

Regarding the rejection of the dependent claims 2-4, applicant submits that the dependent claims 2-4 all depend, directly or indirectly, from independent claim 1, and thus are also patentable over the cited art for at least the reasons discussed above.

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Similarly, claims 20 and 28 have been amended to provide a method (claim 20) and a circuit (claim 28) where a new profile is obtained in response to a new nominal frequency. Applicant submits that Hardin cannot anticipate claims 20 and 28 because Hardin fails to teach an element of the invention, namely obtaining a profile for a new nominal clock frequency.

Regarding the rejection of claims 20, 22-26, 28, 30-33, 35, 37-42, 44-47, 49-54, 59, 61-66, 71-81, and 84-86 under 35 U.S.C. 102(a) as being anticipated by Paist, Applicant submits that Paist fails to teach an element of the present invention, namely obtaining a profile for a new nominal clock frequency.

Applicant submits that Paist discloses a clock generating circuit with a plurality of spreading profiles for ONE nominal clock frequency. Paist is silent with respect to the change in nominal clock frequency (since Paist discloses circuits with only one nominal clock frequency), thus is further silent with the changing of the profile when the nominal clock frequency changes.

With respect to claims 20 and 28, applicant submits that Paist cannot anticipate these claims because Paist fails to teach an element of the invention, namely obtaining a profile for a new nominal clock frequency.

With regard to claim 25, applicant submits that Paist discloses that the profile may be changed on demand for a given application (Col. 8, lines 14-16), meaning the profile memory can be changed for a different application, not for a different nominal clock frequency. Applicant thus submits that this disclosure does not teach that the profile memory is updated while the PLL is generating the clock signal. Paist discloses that the circuit comprises a plurality of spreading profiles where a select signal can select one of them (Col. 3, lines 29-30). Thus applicant submits that the profile changes following Paist's disclosure is not that the profile memory is being updated, but instead another spreading profile is being selected.

With regard to claim 26, applicant submits that Paist is silent with respect to the clock generating circuit with more than one nominal clock frequency. Paist teaches that the nominal frequency changes following the triangular spreading profile from the nominal frequency to a minimum frequency (Col. 6, lines 4-9). As shown in Fig. 3, applicant

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submits that the spreading profile of Paist covers the frequency range from the nominal frequency f_{NOM} to the minimum frequency f_{MIN} following a triangular profile. Thus Paist discloses that the clock signal varies within the spreading profile (nominal frequency f_{NOM}, with a spreading frequency $\Delta f = f_{NOM} - f_{MIN}$) and not that the nominal clock frequency changes from one nominal frequency f_{NOM1} (with a spreading frequency Δf_1) to another nominal frequency f_{NOM2} (with another spreading frequency Δf_2).

With regard to claims 35 and 47, Applicant submits that Paist discloses a clock generating circuit with only one nominal clock frequency since Paist is silent with respect to circuit with different nominal frequencies. Thus Paist fails to teach that the circuit changes nominal clock frequency, and also changes spreading profiles accordingly to improve circuit conditions, e.g. optimizing EMI emission.

Applicant submits that Paist discloses a circuit with a spreading profile (Col. 3, lines 29-30), and applicant also submits that Paist only discloses one nominal frequency. Thus Paist does not disclose that the circuit can have different profiles for different nominal frequencies.

With regard to the examiner's argument that Paist discloses that the spreading profile may be changed on demand for a given application (Col. 8, lines 5-17), applicant submits that Paist teaches that the profile memory can be changed for different applications, not for different nominal clock frequency. Further, by changing spreading profile for a given application, this implies a static switching of the spreading profile, since changing applications normally occurs at the design stage, not at run time.

With regard to claims 40, 52 and 64, applicant submits that the switching is for different nominal frequency.

With regard to claims 41, 53 and 65, applicant submits that Paist discloses a clock generating circuit with only one nominal clock frequency since Paist is silent with respect to circuits with different nominal frequencies. Thus Paist fails to teach that the circuit changes nominal clock frequency, and also changes spreading profiles accordingly to improve circuit condition, e.g. optimizing EMI emission.

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With regard to claim 59, applicant submits that Paist discloses a clock generating circuit with only one nominal clock frequency since Paist is silent with respect to circuits with different nominal frequencies. Thus Paist fails to teach that the circuit changes nominal clock frequency, and also changes profiles accordingly.

With regard to claims 71 and 75, applicant submits that Paist discloses a clock generating circuit with only one nominal clock frequency since Paist is silent with respect to circuits with different nominal frequencies. Thus Paist fails to teach that the circuit slews from one nominal clock frequency to another nominal clock frequency using the first profile.

With regard to claims 72, 76 and 80, applicant submits that Paist discloses a clock generating circuit with only one nominal clock frequency since Paist is silent with respect to circuits with different nominal frequencies. Thus Paist fails to teach that the circuit slews from one nominal clock frequency to another nominal clock frequency using the first profile.

With regard to claims 73, 77 and 81, applicant submits that Paist discloses a clock generating circuit with only one nominal clock frequency since Paist is silent with respect to circuits with different nominal frequencies. Thus Paist fails to teach that the circuit slews from one nominal clock frequency to another nominal clock frequency in a substantially linear variation with respect to time.

With regard to claims 74 and 82, applicant submits that Paist discloses a clock generating circuit with only one nominal clock frequency since Paist is silent with respect to circuits with different nominal frequencies. Thus Paist fails to teach that the circuit slews from one nominal clock frequency to another nominal clock frequency with corresponding profiles.

With regard to claim 79, applicant submits that Paist discloses a clock generating circuit with only one nominal clock frequency since Paist is silent with respect to circuits with different nominal frequencies. Thus Paist fails to teach that the circuit slews from one nominal clock frequency to another nominal clock frequency using the first profile.

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Regarding the rejection of the other dependent claims, applicant submits that these dependent claims all depend, directly or indirectly, from the independent claims, and thus are also patentable over the cited art for at least the reasons discussed above.

Regarding the rejection of claims 35, 41, 47, 53, 59, and 65 under 35 U.S.C. 102(e) as being anticipated by Sha, applicant has amended the claims. Specifically, claims 35 and 47 have been amended to include a limitation that the profile memory is capable of being updated while the PLL is generating the clock signal.

Applicant submits that Sha discloses a ROM memory to store the sets of codes (read a set of spreading profiles), thus fails to teach an element of the present claim, which is a memory capable of being updated while the PLL is generating the clock signal. Further, Sha teaches away from the invention by stating that using a ROM memory to store a set of codes will compromise the overall performance since best performance is achieved only for a few selected frequencies.

Certain embodiments of the present invention provide a solution capable of achieving best overall performance. Since the memory is dynamically updatable, best performance can be achieved for all nominal clock frequencies, since a new best spreading profile for a particular nominal clock frequency can be uploaded into the memory. Also, since the memory is updatable, the memory size can be small. The needed spreading profiles can always be uploaded into the memory, thus eliminating the need for storing all the possible spreading profiles.

Regarding the rejection of the dependent claims 41, 53, 59 and 65, applicant submits that these dependent claims all depend, directly or indirectly, from independent claims 35 and 47, and thus are also patentable over the cited art for at least the reasons discussed above.

Claim Rejections - 35 U.S.C. §103

The Office Action rejected claims 7-8, and 12-16 under 35 U.S.C. 103(a) as being unpatentable over Hardin in view of Paist.

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The Office Action rejected claims 21, and 29 under 35 U.S.C. 103(a) as being unpatentable over Paist as applied to claim 20 above.

The Office Action rejected claims 34, 27, 44-46, 56-58, 68-70, 83 and 88 under 35 U.S.C. 103(a) as being unpatentable over Paist as applied to claim 20 or 26 or 35, 41 or 47, 53 or 59, 65 or 79 or 83 above.

The Office Action rejected claims 36, 43, 48, 55, 60 and 67 under 35 U.S.C. 103(a) as being unpatentable over Sha as applied to claim 35 or 35 and 41 or 47 above, and further in view of Parikh (U.S. Patent No. 7,061,331).

The Office Action rejected claims 82, and 87 under 35 U.S.C. 103(a) as being unpatentable over Paist as applied to claim 79 or 83 above.

Response to Claim Rejections - 35 U.S.C. §103

Regarding the rejection of claims 7-8 and 12-16 under 35 U.S.C. 103(a) as being unpatentable over Hardin in view of Paist, applicant submits that both Hardin and Paist are silent with respect to the clock generating circuit changing from a nominal clock frequency to another nominal clock frequency. Hardin discloses a clock generating circuit providing two close nominal clock frequencies, and Paist discloses a clock generating circuit providing a plurality of spreading profiles for one nominal clock frequency.

Thus applicant submits that both Harding and Paist are silent with respect to an aspect of the present disclosure, namely the optimization of EMI when the clock frequency changes, for example, higher frequency for better performance, or lower frequency for heat reduction or power preservation. Thus applicant submits that changing spreading profile in response to a change in nominal frequency to achieve improve EMI is novel and not rendered obvious over Hardin and Paist.

Further, the argument present above with respect to claim 1 is also applicable to this claim.

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Regarding the rejection of the dependent claims 7-8 and 13-16, applicant submits that these dependent claims all depend, directly or indirectly, from independent claims 1 and 12, and thus are also patentable over the cited art for at least the reasons discussed above.

Regarding the rejection of claims 21, and 29 under 35 U.S.C. 103(a) as being unpatentable over Paist as applied to claim 20 above, applicant submits that these dependent claims all depend, directly or indirectly, from independent claims 20 and 28, and are thus also patentable over the cited art for at least the reasons discussed above.

Regarding the rejection of claims 34, 27, 44-46, 56-58, 68-70, 83 and 88 under 35 U.S.C. 103(a) as being unpatentable over Paist as applied to claim 20 or 26 or 35, 41 or 47, 53 or 59, 65 or 79 or 83 above, applicant submits that these dependent claims all depend, directly or indirectly, from independent claims 20 and 28, and thus are also patentable over the cited art for at least the reasons discussed above.

Further, with respect to claims 44-46, applicant submits that these claims at least provide the scenario or conditions for the present clock generating circuit to change nominal frequency. Applicant submits that Paist fails to teach the EMI optimization when the clock generating circuit changes its nominal frequency.

Regarding the rejection of claims 36, 43, 48, 55, 60 and 67 under 35 U.S.C. 103(a) as being unpatentable over Sha as applied to claim 35 or 35 and 41 or 47 above, and further in view of Parikh, applicant submits that these dependent claims all depend, directly or indirectly, from the independent claims, and thus are also patentable over the cited art for at least the reasons discussed above.

Regarding the rejection of claims 82, and 87 under 35 U.S.C. 103(a) as being unpatentable over Paist as applied to claim 79 or 83 above, applicant submits that these dependent claims all depend, directly or indirectly, from the independent claims, and thus are also patentable over the cited art for at least the reasons discussed above.

Allowable subject matter

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The examiner objected to claims 5-6, 9-11, and 17-19 as being dependent upon a rejected based claim, but would be allowable if rewritten in independent form including all the limitations of the base claim and any intervening claims.

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Response to allowable claims

Applicant submits that these dependent claims all depend, directly or indirectly, from the independent claims, and thus are also patentable over the cited art for at least the reasons discussed above.

Applicant respectfully requests that a timely Notice of Allowance be issued in this case. If there are any additional charges, please charge Deposit Account No. 02-2666.

Respectfully submitted,

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